Virtual Display – Validation IP core Product Brief

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Overview

The **Virtual Display IP** is a Validation IP core designed to enable automated testing of the output of display controllers with DPI-2 output interface. While visual inspection of display output may be appropriate during the development phase, it is not a viable approach when setting up an automated validation environment. The Virtual Display IP receives the display output signal and writes it to system memory. The content of the system memory can then be accessed via a software API for further evaluation and tests on CPU side.
The IP core has been designed for use in FPGA validation environments.

Specification

Concept and functionality

It is not uncommon for designs implemented on an FPGA during validation to exhibit lower maximum frequency (f_{max}) values than those observed in their ASIC implementations. Therefore, it is not possible to validate video modes with high pixel clock frequencies, such as Full HD and 4K UHD, with a real display.

The Virtual Display IP can be connected to a DPI-2 interface of a display controller. It will then synchronize with the frame start and write all video data, including the sync signals (e.g. hsync), to a buffer via an AXI bus master.
The captured data is simply written to the buffer in the same order it is captured. The number of bytes written depends on the width and height of the frame and the capture mode. Depending on the capture mode, the data will contain the front and back porch period and the horizontal blank period.
The video data can then be inspected by software tools, for example by comparing it with a reference image or by carrying out sanity checks on the sync signals.

Limitations

- Max. frame size is 4096*4096 visible pixels.
- Buffer format is XRGB8888.
  - However, color formats with bit widths below 8 can still be used. Unused bits are simply set to '0'.
- Design is optimized for implementation on Altera FPGAs.
  - Note: Support for other FPGA types can be discussed.

Deliverables

IP Core

- The IP core is delivered (for Altera FPGAs) as an encrypted Quartus Platform Designer Component (Qsys component).
  - Note: Optional delivery as VHDL source code can be discussed.

Software

- Bare Metal ANSI-C Driver
  - Easily adaptable backend for any bare metal system.
  - Linux Kernel backend

- Linux Example application
    - Simple example application for Linux that uses the driver API to capture a frame

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