Overview

The Controller Area Network (CAN) is a highly reliable serial bus protocol defined in the Bosch CAN specifications for standard CAN 2.0B and CAN FD, as well as ISO 11898-1:2024.
The TES CAN Flexible Data-Rate Controller IP core is a Hardware IP core written in VHDL. The core is intended for use in a System-on-Chip (SoC) environment. It can be integrated into a wide range of applications and target technologies. The code is synthesizable for Application Specific Integrated Circuits (ASIC) and Field Programmable Gate Arrays (FPGA).

Features

- CAN 2.0B protocol compatible (ISO 11898-1).
- CAN Flexible Data-Rate (FD) protocol compatible (ISO 11898-1:2024).
- Supported Frame Formats:
  - CAN Base: 11-bit Identifier and constant bit rate.
  - CAN Extended: 29-bit Identifier and constant bit rate.
  - CAN FD Base: CAN Base format with dual bit rate.
  - CAN FD Extended: CAN Extend with dual bit rate.
- Data rates:
  - Up to 1 Mbit/s for CAN 2.0B.
  - Up to 8 Mbit/s for CAN FD.
- Payload sizes:
  - CAN Base/Extended: 0...8 bytes.
  - CAN FD Base/Extended: 0…64 bytes.
- Clock Prescaler provides a wide frequency range.
- Flexible interface configurations.
- RX frame filter.
- Bosch CAN Reference model certified for CAN 2.0B functionality.
- CAN 2.0B functionality certified for aviation-related applications.
- CAN FD functionality working in FPGA application.
- CAN FD in Silicon Q1’25.

Technology Details

MAC Device

The TES CAN FD Controller IP core is a device positioned in the OSI model in the Medium Access Control (MAC) sublayer section of the Data Link Layer (Layer 2).

The main tasks of an MAC layer device are:

- Message framing.
- Transmission and reception of frames.
- Arbitration.
- Error detection and signaling.
- Fault confinement.
- Bit timing and synchronization.

Logical Link Control (LLC) Support

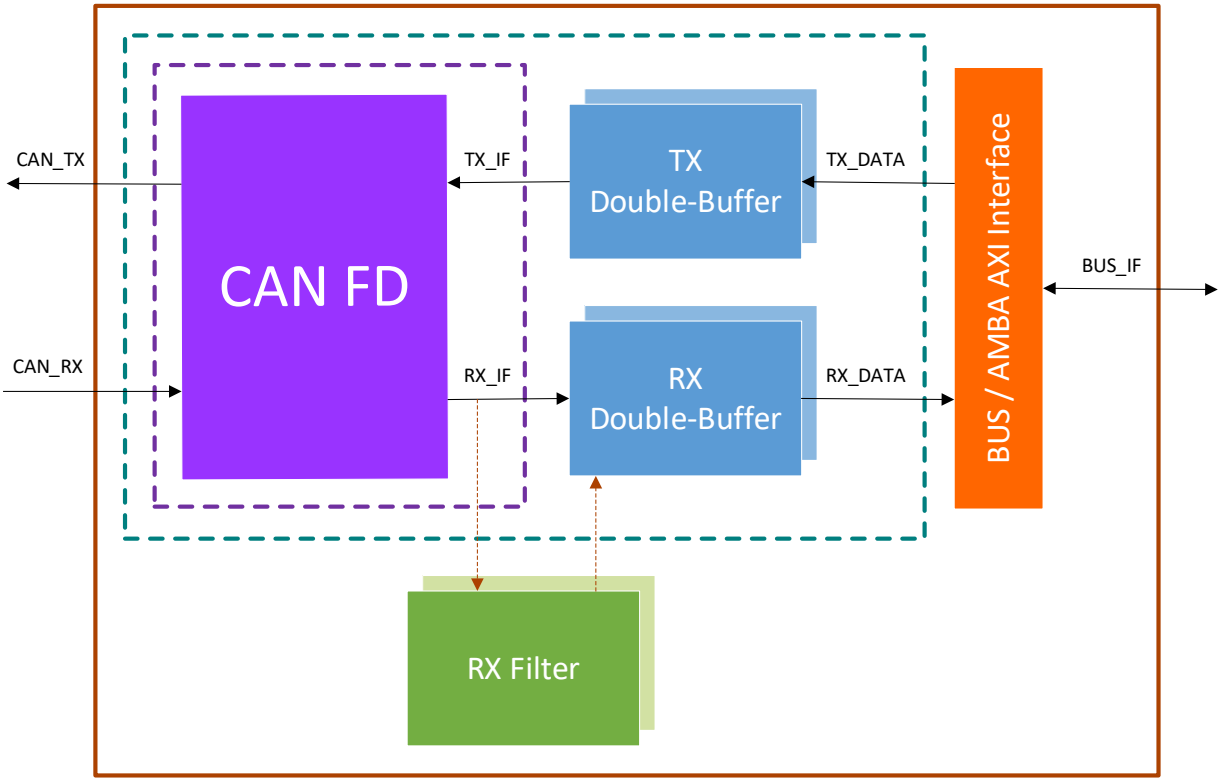
To achieve a high application flexibility for this core, the acceptance filtering and buffering of received messages is provided for Logical Link Control (LLC, part of layer 2 of the OSI model) sublayer application support, which may be implemented using hardware, software, or a combination of both.

Interface Configurations

The TES CAN FD Controller IP core can be integrated into SoC device or other applications using one of the following configurations:

- Core interface with a memory interface.
- Core interface double buffers for transmit and receive. Data interface to the double buffers.
- BUS / AMBA AXI interface for access via internal SoC bus.

The RX Filter can be added in each variant.



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