Overview

D/AVE NX is the latest and most powerful addition to the D/AVE family of rendering cores. It is the first IP to bring full OpenGL ES 2.0/3.1 rendering to the FPGA and SoC world. Targeted for graphics user interfaces on displays up to 4K x 4K resolution in the Industrial, Medical, Military, Avionics, Automotive and Consumer markets D/AVE NX is designed to meet the sweet spot of performance and footprint.

By enabling the use of state of the art shader based APIs even on small devices high quality 2D and full 3D applications can be satisfied using the D/AVE NX core. The possibility to work with a modern language like OpenGL ES 2.0/3.1 enables the user to rapidly build high-end user interfaces (e.g. based on QT or Android) and makes new, future proof implementations possible. D/AVE NX can scale easily to fit exactly into the resource/performance sweet spot for a particular application. Entire device families can be equipped with differently scaled variants of the core, making all of them fully software compatible. A single unified software stack and the guarantee to produce the exactly same visual result (at different speeds) allows saving significant development resources.

D/AVE NX is highly efficient as the internal multi-level scheduler can maximize the utilization of every HW element even better than the fixed function pipeline of the successful D/AVE cores could. Scheduling also does not have to be pre-computed in the compiler simplifying the compiler and driver architecture considerably.

Technology Details

System Features

- Scalability throughout the entire design
  - Scaling from tiny footprint up to high end performance
  - Scalable unified shader architectures are a perfect fit for FPGAs
  - Exact same driver / software stack can be used on all versions
  - Enables the same output at different speeds
- Unified Shader Architecture
  - Dynamic, fully reconfigurable shaders
  - Efficient support for branches / divergent control flow
  - Fully IEEE compatible floating point ALUs (incl. rounding, denormals etc.)
  - Compressed shader binaries for higher code density
  - Non-constant varying indexing
  - True integer arithmetic (8bit, 16bit, 32bit)
  - Multi level caches for shader memory
- Massively parallel execution with fine grained Multithreading
  - Thread context switch near instantaneous (~2 cycles)
Advanced task scheduler supporting both long and short term stalls
- Architecture is able to eliminate hundreds of cycles of latency
- Concurrent use from multiple applications
- Job preemption possible on fragment level

Bandwidth reduction techniques
- On the fly lossless data compression/decompression
- Sophisticated caching mechanisms

Application optimization and debugging support
- Multiple hardware performance counters
- Detailed analysis of shader stalls and scheduling

Pipelined architecture for high clock frequencies

System security features
- Stop on bus error for integration with memory protection units
- Hardware out-of-framebuffer memory access protection

Rendering
- Full support of all OpenGL ES 2.0/3.1 and VULKAN rendering features
- High render quality
  - Highly accurate sub pixel positioning, interpolation and filtering
  - Multiple anti-aliasing techniques (including MSAA)
- Effective texture compression
  - Multiple high quality standard codecs ETC2/EAC, ASTC
  - Maximizing the visual quality with a given bandwidth
  - Saving storage and transfer resources
- Hardware supported blending
  - Normal alpha blending
  - Linear colorspace blending
  - Porter-Duff blending (alpha premultiply / postdivide)
- Various texture and framebuffer formats
  - 8 bit alpha/luminance, ARGB4444, ARGB1555, RGB565, ARGB8888 etc.
  - Wide formats with up to 128bit per pixel
  - Floating point texture support
  - 3d Texture and texture array support
  - Easily extendable
- High resolutions
  - Frame buffers and textures up to 4k x 4k pixels
- Support for Image Transformation & Warping
- Composition Engine

Power Management
- Memory blocks controlled by Chip Select port
- Prepared for efficient automatic clock gating
- Global clock gating as option
Integration
- Low resource consumption (starting at 31K LE)
- Single clock domain architecture
  - Bus interface clock frequency may differ from core frequency
- High latency capable
- Optional internal arbitration to work with a single bus master
- Adaptors for common bus protocols
  - ARM AMBA: APB for register access, AHB or AXI (preferred) for memory bus master access
  - Intel PSG Avalon as bus adaptors for both register and bus master access
  - Other bus protocols can be easily adapted

Resource Usage
The actual resource usage of D/AVE NX depends mainly on the number of Shader Units (SUs), the number of Arithmetic Logic Units (ALUs) per shader unit and partly on the bus and cache configuration.

Verification Concept
A 100% algorithmic equivalent C model is used as reference for the verification of the RTL code. This real-time capable reference model is called ‘Soft D/AVE’ which acts as a pixel accurate emulator on Windows PC. The emulator is also used for driver and application development.

The following test metrics are used:
- Functional Coverage
- Code Coverage using Cadence IUS
- Static Code Analysis
- Timing Checks
- FPGA prototyping
Software

Drivers
TES provides Khronos conform OpenGL ES 2.0/3.1 and EGL drivers. Both drivers rely on a low level D/AVE NX driver layer abstracting hardware details like the register access and making porting to different CPUs / Operating systems a lot easier.

All drivers have the following features:
- Fully reentrant & thread-safe
- Minimal OS dependency (HAL part separated)
- No inline assembler required
- Support for multiple D/AVE NX instances
- Multi-threading support, i.e. multiple applications can use D/AVE NX concurrently
- Small memory footprint

![Diagram](image_url)
D/AVE NX reference Qt system solution on Yocto-Linux

TES delivers a complete reference system solution for Intel PSG SoCs supporting selected reference boards (e.g. D10-Nano SoC board featuring Cyclone 5 SoC) including:

- Qt 5.x
- Yocto Linux OS
- OpenGL ES 2.0 and EGL drivers for D/AVE NX and CDC-200NX as source code
- Qt and native OpenGL ES 2.0 example applications as source code
- Build scripts to check out required repositories (Yocto-Linux, Qt, meta layers, drivers,...) and build the D/AVE NX demo SD card image as well as the complete SDK.
- D/AVE NX as Megacore IP block (QSys component)
- CDC-200NX Display Controller as Megacore IP block (QSys component)

The delivered package includes everything to evaluate the IP and start an own integration and application project.

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